So You Think You Cannot Test Your PCB?

- PCB with limited or no physical test point access?
- Nets with controlled impedance?
- Test pads too small?
- Net count so high it exceeds the capability of conventional ICT?

Manufacturing defects are becoming more and more difficult to detect. In-Circuit test is reaching the limits of its usefulness on RF, high speed or large PCBs. Boards with 5,000 nets. 2,000 pin BGA devices. Analog components the size of a pin head. All these things are changing the way that Test Engineers approach the testing their PCBs.

Agilent began addressing the issue of test access with their introduction of Silicon Nails and Magic Test. Silicon Nails is a method by which virtual test points are created on digital net where there is no physical access. Magic Test is a method of calculating the bulk DC & AC impedance of an analog circuit and creating a test that will confirm the existence of the components. The limitation of these two methods is that they still require a significant amount of physical test point access to be effective. This does not even address the non-recoverable expenses of the test fixture and test program. High density boards with small test points can have fixture costs ranging as high as $60,000.00 or more.

Enter the modern flying probe test system. These are not the flying probe testers of just a few years ago. The manufacturers of this new generation have expanded the test capabilities and leveraged the limitations of flying probe systems to rival the coverage achieved with an in-circuit tester. What was a tester used for prototype and very limited production boards has become a frontline manufacturing test system. The greatest advance in the flying probe testers is in the area of digital fault detection. Opens, high impedance shorts and damaged IO structures are all detectable using the flying probe testers. Some of these failures cannot be detected by in-circuit testers. Interestingly you do not need to apply power to detect these faults on a flying probe tester. The downside of these advances in test capability is the increased test time that each increment of test coverage costs. This is not the seconds and minutes of test time at in-circuit test, but quite possibly hours of test time per PCB

Enter the modern Boundary Scan test system. With access to only 5 signals nets and power a boundary scan test system can test the interconnectivity of boundary scan devices, surrounding interconnect logic, memory and analog components. Programming of CPLDs, FPGAs and Flash Memory devices can also be done through the boundary scan interface. Test time for boundary scan is seconds rather than the minutes and hours of flying probe.

So what you say? Imagine that a full featured flying probe test program for your 5,000 net PCB will cost, on a per unit basis, $250.00. Explaining that cost to be added to the

base cost of your $2,500.00 PCB, an increase of 10%, to the operations staff might be uncomfortable.

So how do you lower the cost of test without losing test coverage? Leverage your board design. Perform a limited subset of flying probe testing followed by boundary scan testing of the active components. By reducing the amount of time spent at flying probe test the overall test cost can be reduced by as much as 50%. The test coverage at flying probe can be targeted based upon the test coverage achieved with the boundary scan test system. In addition the development process for the flying probe program would include the full featured test plan. This full test plan would be used as a troubleshooting aid for boards that have passed the previous hybrid flying probe and boundary scan test but fail at functional test.